

Compact Submillimeter-wave Receivers made with Semiconductor Nano-Fabrication Technologies

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Abstract — Advanced semiconductor nanofabrication techniques are utilized to design, fabricate and demonstrate a super-compact, low-mass (<10 grams) submillimeter-wave heterodyne front-end. RF elements such as waveguides and channels are fabricated in a silicon wafer substrate using deep-reactive ion etching (DRIE). Etched patterns with sidewall angles controlled with 1° precision are reported, while maintaining a surface roughness of better than 20 nm rms for the etched structures. This approach is being developed to build compact 2-D imaging arrays in the THz frequency range.

Index Terms — Silicon micromachining, nanotechnologies, deep-reactive ion etching, surface roughness, super-compact receiver front-ends.

I. INTRODUCTION AND BACKGROUND

Submillimeter-wave heterodyne receivers are important for a number of applications, from providing quantitative molecular abundance profiles in atmospheres [1] to detection of contra-band and IEDs [2,3]. The current generation of receivers relies on metal waveguide blocks made using conventional precision machining tools such as end mills. For real time imaging capabilities and for large fields of view it is highly desirable to have two dimensional detector arrays, and therefore novel approaches to building compact waveguide architectures are needed.

Here we demonstrate that advanced semiconductor nanofabrication technologies can be used to build a compact 530-590 GHz receiver front-end in an all-silicon waveguide structure. The wafers are processed using deep reactive ion etching (DRIE) techniques [4] to form channels for mounting low-parasitic GaAs Schottky diode chips [5] and custom waveguide matching circuits for coupling THz power both laterally and vertically with low return loss. We also report the ability to etch silicon waveguides with precisely controlled vertical angles, which may enable the integration of high-performance all-silicon conical beam horns for coupling energy to and from free space.

II. MICROMACHINING OF SILICON

The utilization of micromachined silicon for THz circuits places a number of important constraints on the structures.

First, THz frequency waveguides and device channels need very smooth sidewalls and bottom surfaces in order to minimize ohmic losses. The cross sections of the waveguide walls also have to be precisely rectangular in order to minimize scattering from geometric inhomogeneities and integrate MMIC amplifiers, multipliers, and mixers successfully. Finally, a robust and accurate alignment scheme is needed to assure good impedance matching across vertical wafer-to-wafer waveguide transitions.

Silicon wafers are processed with conventional UV lithography, and Deep Reactive Ion Etching (DRIE) techniques using thick AZ9260 resist as etching mask. The DRIE technique used is the well-known Bosch process based on the alternative exposures to SF₆ and C₄F₈ gases [6]. With optimized plasma power and etching gas ratios, we can achieve a selectivity of 50:1 for etching at low rates (2 $\mu\text{m}/\text{min}$) and up to 75:1 for long and deep etches (4 $\mu\text{m}/\text{min}$).

II.1 – ETCHED PATTERN SURFACE ROUGHNESS

To avoid losses during signal transmission due to high silicon peaks at the bottom of the etched patterns, they must have a surface roughness better than 50 nm [7]. With these smooth surfaces, the excess noise coming from the surface roughness should be negligible compared to the total ohmic losses [8]. As shown in Figure 1, our optimized DRIE process can achieve an 18 nm rms surface roughness on the bottom of a 280x280x40 μm waveguide channel etched in a 500 μm thick silicon wafer.

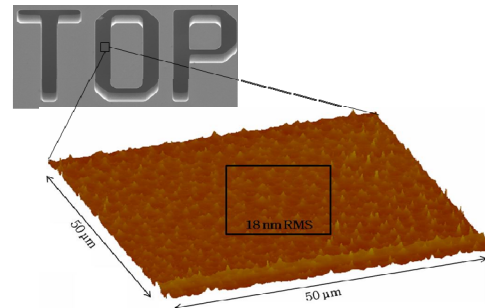


Fig. 1: AFM measurement of silicon micromachined waveguides indicates that 18 nm rms surface roughness can be achieved.

During the DRIE Bosch process, the SF_6 is used to etch the silicon, while the C_4F_8 passivates the etched surfaces. This alternation of etching and passivation steps results in anisotropic etch of the silicon and it can modulate the sidewall profile. With the control of the gas flows and pressures, this scalloping effect can be significantly reduced. To achieve the small levels of surface roughness shown in Figure 1, a specific etching recipe was developed with a ramp up of the plasma power during the etch cycle, instead of keeping it constant. Figure 2 compares two similar waveguides, both $500\text{ }\mu\text{m}$ x $300\text{ }\mu\text{m}$ and $100\text{ }\mu\text{m}$ deep.

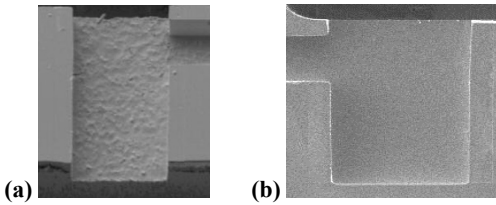


Fig. 2: Fixed plasma power (a) vs ramping up during etching (b) results in better surface quality of the waveguide structures.

II.2 – SIDEWALL SMOOTHNESS AND VERTICALITY

In addition to the surface roughness issue, the etched sidewalls must be very smooth and perpendicular to the top surface with a maximum error of 1° . This is to ensure two important criteria: first, pattern size variations will affect the characteristic impedance, and second, accurate alignment between wafers depends on the high tolerances of the dowel pin/hole mating structures we use. Figures 3 and 4 show how changing the ratio “etching” vs “passivation” can improve the sidewall quality.

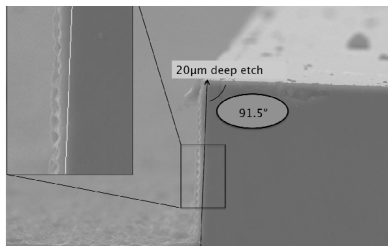


Fig. 3: SEM picture of an etch pattern with the Bosch effect on the sidewall, where scalloping is visible.

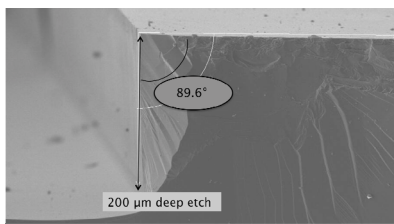


Fig. 4: SEM picture showing the improvement of the sidewall smoothness and angle by modifying the etching and passivation steps duty cycles.

While vertical sidewall profiles are important for waveguides, some RF structures such as horns need sidewalls with controlled slopes. For example, submillimeter-wave Pickett-Potter feed horns are widely used for submillimeter-wave components. The typical Pickett horn has a slope of 13.5° but this angle can be reduced to 5° , if the total height of the horn is redesigned to control the sidelobes of the propagation modes^[9,10]. Figure 5 shows two SEM pictures of DRIE patterns with intentionally angled sidewalls of 5° and 8° from normal. These angles can be obtained by addition of power ramps and various cycle times of etching / passivation steps. We plan to use this novel micromachining approach to fabricate and test integrated Pickett-Potter horns as silicon-based antennas.

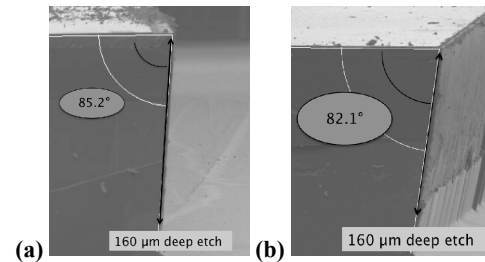


Fig. 5: DRIE etched patterns with 5° (a) and 8° (b) sidewall vertical angles.

II.3 – PRECISE WAFER-TO-WAFER ALIGNMENT

A technique using circular etched pockets and silicon donuts-shaped dowel pins has also been developed to align two wafers together. The donut shape was selected to prevent trapped air under the silicon pin during the assembly and to make it easier to handle with tweezers. An optical and SEM photographs are shown in Figure 6. With this technique, we can achieve a $5\text{ }\mu\text{m}$ alignment or better, so small silicon pieces working at high frequencies.

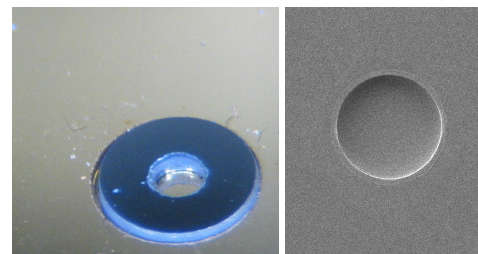


Fig. 6: Silicon donuts and etched pockets are used to achieve precise wafer-to-wafer alignment.

III. 560GHZ RADIOMETER-ON-A-CHIP

Utilizing the silicon nanofabrication techniques discussed above, a super-compact 560 GHz receiver front-end has been designed, fabricated and tested. A three dimensional diagram of the receiver stack is shown in Figure 7.

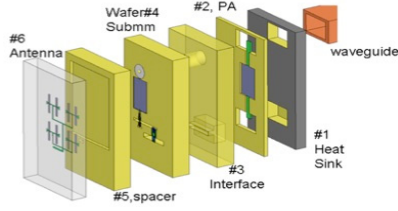


Fig. 7: Stack of silicon wafers comprising a submillimeter-wave receiver front-end. The LO signal from the input waveguide is amplified, multiplied and mixed with the RF signal from the antenna.

The first and second stages of this receiver-on-a-chip (ROC) feature a W-band power amplifier (PA) MMIC packaged in a silicon micro-machined block. The transitions are chosen to have the input/output waveguide interfaces with external waveguides on the flat surface of the wafers^[11]. An SEM picture of the fabricated Si-based W-band amplifier (showing the channel where the MMIC will be placed) is shown in Figure 8.

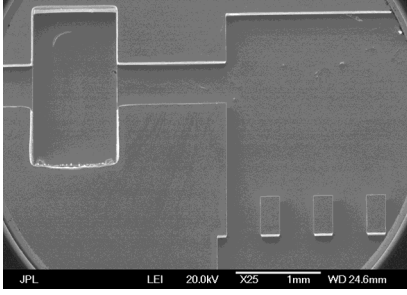


Fig. 8: SEM picture of a Si-based W-band amplifier, showing a double-step etch 280um-115um.

The third and fourth stages of the ROC feature an integrated 265-300 GHz tripler and 530-600 GHz sub-harmonic mixer using MMIC planar Schottky diode devices. These two stages require 4 silicon pieces and nine DRIE etches with depths ranging from 20um to 750um (etch-through). SEM pictures of the fabricated waveguides and cavities for stages 3 and 4 are shown in Figure 9. These silicon pieces were fabricated before those presented previously in part II, and therefore the bottom of the etched patterns is very rough.

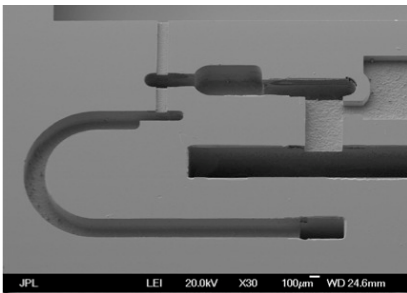


Fig. 9: SEM picture of Si-based etched cavities and waveguides fabricated for the 560 GHz Radiometer-On-A-Chip architecture.

IV - MEASUREMENT SETUP AND RESULTS

The first and second stages of the ROC were tested first in order to measure the amount of output power available at W-band to pump the following stages. The performance of the W-band amplifier module is shown in Figure 10. Using a conventional metal machining pre-amplifier cascaded with a silicon packaged MMIC power amplifier, an output power of 40-140 mW was measured between 92 and 104 GHz.

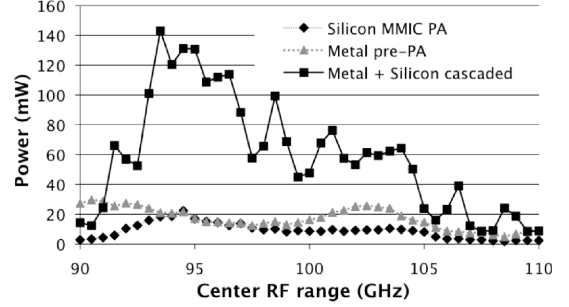


Fig. 10: Measured performance of the 1st and 2nd ROC stages featuring a W-band metal pre-amplifier and silicon-based power amplifier MMICs measured separately (lower curves) and cascaded (top curve).

The third and fourth stages of the ROC have been tested using a fundamental LO source consisting of an Agilent E8257D synthesizer, an Agilent 83558A W-band source, a W-band pre-amplifier stage and a W-band rotary vane attenuator. As shown in Figure 11, preliminary results give a DSB mixer noise temperature of 4860 K and DSB mixer conversion losses of 12.1 dB at 540 GHz.

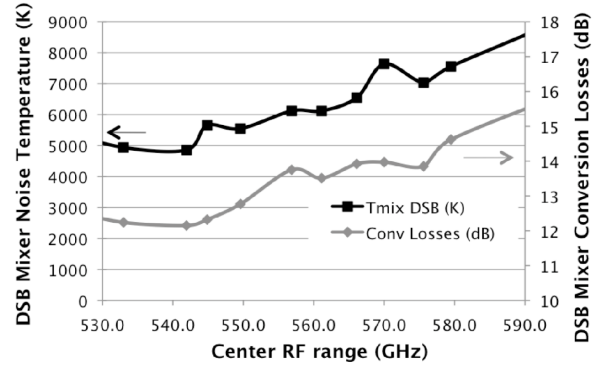


Fig. 11: Preliminary measured performance of the 3rd and 4th ROC stages showing the DSB mixer conversion losses (top curve) and noise temperature (bottom curve) VS central RF range.

Simulated results with a 20 nm rms surface roughness suggest that the mixer performance should be better by about 3 dB. But, as mentioned before, the silicon pieces used for these measurements were very rough, so we can in part attribute these worse than expected results to that high surface roughness. Nonetheless, the receiver performance of Figure 11 provides proof of concept that nanofabrication technologies

can be utilized to make compact and low-mass submillimeter-wave receiver front ends.

Recently, new silicon waveguide structures have been fabricated using the DRIE recipes reported in part II. In the SEM picture shown in Figure 12, etched cavities and waveguides have the 18 nm rms smooth surface.

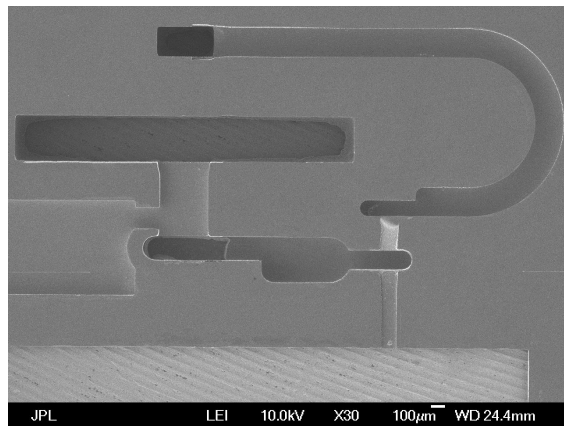


Fig. 12: SEM picture of improved Si-etched cavities and waveguides for the 560GHz Radiometer-On-A-Chip architecture.

IV. CONCLUSION

A conceptual design for a super compact submillimeter-wave receiver is presented. The technique utilizes nanofabrication technologies such as wafer bonding and silicon micromachining techniques to achieve receiver front-ends that are low mass and low volume. A prototype W-band power amplifier module and a 530-590 GHz receiver front end, both silicon-based, have been demonstrated. This technique provides the flexibility of building a radiometer-on-a-chip and opens up possibilities for large format array receivers, multi-frequency imaging arrays, and beam-steering capabilities for future heterodyne array receivers.

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